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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	11

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/399,510	Applicant(s) DONG ET AL.	
	Examiner Justin P Misleh	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 3, 5 - 7, 9, and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 3, 5 - 7, 9, and 10* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In the Non-Final Office Action (Paper No. 9, 26 Feb. 2004), the Examiner brought to the attention of the Applicant that the listing of references in the specification was an improper information disclosure statement and unless cited by the Examiner on form PTO-892, the references have not been considered. The Applicant did not address this issue in the Amendment. The Examiner has repeated the concern in the paragraphs below.

2. Applicant's arguments filed 8 March 2004 have been fully considered but they are not persuasive.

The Applicant initially states, "Claims 4 and 8 have been cancelled and their limitations have been incorporated into Claims 1 and 7, respectively." This is true, however, the Examiner notes that the amendments made to Claims 1 and 7 are not limited by only the limitations found in Claims 4 and 8, respectively. For instance, Claim 1 recites therein "a second voltage level different from the said first voltage set level." The above-cited limitation was not previously found in Claim 4 and thus raises new issues. Claim 7 recites a similar limitation that raises new issues.

Since, the Applicant has further limited Claims 1 and 7, the Examiner has chosen to interpret Kim et al. (US 6,597,395 B1) in another light, separate and distinct from the interpretation found in the Non-Final Office Action. Since, the Applicant's arguments pertain to the interpretation of Kim et al. according to the Examiner's interpretation in the Non-Final

Office Action, the Applicant's arguments regarding Kim et al. are moot. Please see the rejections below for the Examiner's new interpretation of Kim et al.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the Examiner on form PTO-892, they have not been considered.

More specifically, US Patent No. 4,187,519 was listed in the specification on page 2 (lines 12) and is not listed in the Information Disclosure Statement (Paper No. 4, 10 January 2000).

Claim Objections

4. **Claim 10** is objected to because of the following informalities: dependency issue.

The claim language recites in the preamble, "The image processor of Claim 7", however, Claim 7 does not introduce an image processor, rather Claim 7 requires an image sensor. For the purposes of examination, the Examiner will interpret the preamble of Claim 10 as, "The image sensor of Claim 7".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 2, 5 – 7, 9, and 10** are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al.

7. For **Claim 1**, Kim et al. disclose, as shown in figure 2 and as stated in columns 3 (lines 7 – 67), 4 (lines 1 – 10), and 5 (lines 1 – 26), a method for auto black expansion in an image sensor (CCD 100), comprising:

(a) comparing (performed in the Digital Comparator – 230) the voltage level of processed pixel signals (CDS/AGC – 200 process the signals by performing correlated double sampling) with a first set voltage level (voltage level B from the microcomputer);

(b) maintaining a first count of a number of pixels signals that are above or below the first set voltage level (Up/Down Counter – 240 raises and or lowers a running count depending upon whether the pixels signals are greater than or less than the first set voltage level; see column 3, lines 65 – 67, and column 4, lines 1 – 4); and

(c) using the count to determine a first digital control signal for adjusting the black level calibration of the processed pixel signals (The Up/Down Counter – 240 and the Digital Comparator – 230 both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter – 240, is applied to the D/A Converter – 250 so as to provide control for a

Black Level Clamp Circuit – 260. The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration.); and

(d) comparing (Black Level Clamp Circuit 260) the pixel signals to a second set voltage level (The second set voltage level is the "divided" voltage value selected from a plurality of divided voltages by the D/A Converter – 250, according to the control signal; see column 3, lines 25 – 27, column 4, line 63 – 68, and column 5, lines 1 – 4) different from said first set voltage level (as will become evident in the explanations below) and maintaining a second count related to the comparison of the pixel signals to the second level (see explanation below).

The whole object of Kim et al. is to establish two different lower phase reference voltages. One lower phase reference voltage (V_B), generated by the reference voltage generator (220), is applied to the A/D Converter (210). The other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2) is established by the D/A Converter (250) and is identified, in figure 2, as the signal output from the D/A Converter (250) and input into the Black Level Clamp Circuit (260). The D/A Converter (250) accepts two inputs: the n-bit control signal output from the Up/Down Counter (240) and the one lower phase reference voltage (V_B). The D/A Converter (250) divides the one lower phase reference voltage (V_B), according to the n-bit control signal, into the other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2).

Regarding the claim language, the processed pixel signals (output from CDS/AGC – 200) are compared in the Black Level Clamp Circuit (260) to the "divided" voltage value output from the D/A Converter (250). The same processed pixel signals (i.e. the processed pixel signals are output from the CDS/AGC – 200) are compared to a first set voltage level (voltage level B) in

the Digital Comparator (230) and then are compared to a second set voltage level ("divided" voltage value) in the Black Level Clamp Circuit (260). Because, Kim et al. disclose a feedback loop to effect Black Level Calibration, a first count is maintained by the Up/Down Counter (240) prior to the generation of the n-bit control signal and a second count is maintained by the Up/Counter Down Counter (240) after generation of the n-bit control signal and comparison to the second set voltage level. In other words, the first count is used to generate the n-bit control signal so as to generate the second set voltage level. The Black Level Clamp Circuit (260) clamps the black level in the processed pixel signals to the second set voltage level. The resultant clamped signal is fed back to the CDS/AGC (200) to become new processed pixel signals. The new processed pixel signals are compared in the Digital Comparator (230) so as to establish a second count relating to the comparison of the processed pixel signals to the second level. Since, the new processed pixel signals are dependent upon the comparison in the Black Level Clamp Circuit (260) to the second set voltage level, the second count using the new processed pixel signals in the Up/Down Counter (240) is related to the comparison.

8. As for **Claim 2**, Kim et al. disclose the method Claim 1, wherein the adjustments to the black level calibration are made in between fields of pixels signals.

The Applicant defines, on pages 2 (lines 16), 3 (lines 15 and 16), 4 (line 3), 8 (line 18), 9 (lines 16 and 17), 10 (lines 21 and 22), and 12(line 1), that a "field of pixel signals" corresponds to an image signal, or rather a "sensed image" or a "scene". Thus, Kim et al. teach that adjustments to the black level calibration are made on image signals, as stated in column 3 (lines 14 – 18), and thus, are made between fields of pixel signals.

9. As for **Claim 5**, Kim et al. disclose, the method of Claim 1, wherein the second count (provided by Up/Down Counter – 240 dependent upon the new processed pixel signals) is used to determine a second digital control signal for adjusting the amplification of the processed pixel signals.

The Up/Down Counter (240) and the Digital Comparator (230) both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter (240), is applied to the D/A Converter (250) so as to provide control for a Black Level Clamp Circuit (260), which in turn further provides control to the amplifier circuit (CDS/AGC Circuit – 200). The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration and amplifying the pixel signals.

10. As for **Claim 6**, Kim et al. disclose, as shown in figure 2, the method of Claim 5, wherein adjustments to the amplification (CDS/AGC Circuit – 200) of the processed pixel signals are only made after adjustments to the black level calibration (Black Level Clamp Circuit – 260) have adjusted the pixel signals to a desired voltage level.

The black level of the pixels signals is adjusted prior to amplification. In other words, it is necessary to adjust the black level of the pixels prior to adjusting the amplification of the pixel signals.

11. For **Claim 7** (see objection above), Kim et al. disclose, as shown in figure 2 and as stated in columns 3 (lines 7 – 67), 4 (lines 1 – 10), and 5 (lines 1 – 26), an image sensor (CCD 100) for processing image signals that are comprised of processed pixel signals, the image sensor comprising:

(a) auto black expansion circuitry for adjusting the relative voltage level of the image signal (The Digital Comparator – 230, Up/Down Counter – 240, D/A Converter – 250, Black Level Clamp Circuit – 260, and CDS/AGC Circuit – 200 are all required for adjusting the black level calibration of the image signals);

(b) a black level voltage input (Black Level Calibration Voltage B, first iteration of the feedback loop);

(c) a comparator (Digital Comparator – 230, first iteration of the feedback loop), the comparator comparing the processed pixel signals (Image Signal A) to the desired black level signal (Black Level Calibration Voltage B, first iteration of the feedback loop);

(d) a counter (Up/Down Counter – 240) for maintaining a count related to the comparison performed by the comparator (Up/Down Counter – 240 raises and or lowers a running count depending upon whether the image signal is greater than or less than the Black Level Calibration Voltage B, first iteration of the feedback loop; see column 3, lines 65 – 67, and column 4, lines 1 – 4); and

(e) a digital controller (D/A Converter – 250) for utilizing the count maintained by the counter to determine desired adjustments to the auto black expansion circuitry (The Up/Down Counter – 240 and the Digital Comparator – 230 both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter – 240, is applied to the D/A Converter – 250 so as to provide control for a Black Level Clamp Circuit – 260. The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration), and

(f) a mid-level voltage input (The mid-level voltage input is the "divided" voltage value selected from a plurality of divided voltages by the D/A Converter – 250, according to the control signal; see column 3, lines 25 – 27, column 4, line 63 – 68, and column 5, lines 1 – 4) different from said black level voltage input (as will become evident in the explanations below) and a second comparator (Black Level Clamp Circuit 260) for comparing processed pixel signals to the mid-level voltage input (see explanation below.

The whole object of Kim et al. is to establish two different lower phase reference voltages. One lower phase reference voltage (V_B), generated by the reference voltage generator (220), is applied to the A/D Converter (210). The other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2) is established by the D/A Converter (250) and is identified, in figure 2, as the signal output from the D/A Converter (250) and input into the Black Level Clamp Circuit (260). The D/A Converter (250) accepts two inputs: the n-bit control signal output from the Up/Down Counter (240) and the one lower phase reference voltage (V_B). The D/A Converter (250) divides the one lower phase reference voltage (V_B), according to the n-bit control signal, into the other of the two different lower phase reference voltages (not labeled but clearly shown in figure 2).

Regarding the claim language, the processed pixel signals (output from CDS/AGC – 200) are compared in the Black Level Clamp Circuit (260) to the "divided" voltage value output from the D/A Converter (250). The same processed pixel signals (i.e. the processed pixel signals are output from the CDS/AGC – 200) are compared to a black level voltage input (voltage level B) in the Digital Comparator (230) and then are compared to a mid-level voltage input ("divided" voltage value) in the Black Level Clamp Circuit (260). Because, Kim et al. disclose a feedback

loop to effect Black Level Calibration, a first count is maintained by the Up/Down Counter (240) prior to the generation of the n-bit control signal and a second count is maintained by the Up/Counter Down Counter (240) after generation of the n-bit control signal and comparison to the mid-level voltage input. In other words, the first count is used to generate the n-bit control signal so as to generate the mid-level voltage input. The Black Level Clamp Circuit (260) clamps the black level in the processed pixel signals to the mid-level voltage input. The resultant clamped signal is fed back to the CDS/AGC (200) to become new processed pixel signals. The new processed pixel signals are compared in the Digital Comparator (230) so as to establish a second count relating to the comparison of the processed pixel signals to the mid-level voltage input. Since, the new processed pixel signals are dependent upon the comparison in the Black Level Clamp Circuit (260) to the mid-level voltage input, the second count using the new processed pixel signals in the Up/Down Counter (240) is related to the comparison.

12. As for **Claim 9**, Kim et al. disclose, the image sensor of Claim 7, further comprising automatic gain control circuitry (200), wherein the digital controller (250) utilizes the count of a second counter to determine adjustments to the automatic gain control circuitry (200).

The Up/Down Counter (240) and the Digital Comparator (230) both accept and output digital signals. An n-bit control signal, provided by the Up/Down Counter (240), is applied to the D/A Converter (250) so as to provide control for a Black Level Clamp Circuit (260), which in turn further provides control to the amplifier circuit (CDS/AGC Circuit – 200). The n-bit digital control signal, provided by the Up/Down Converter – 240, is required for adjusting the black level calibration and amplifying the image signal.

13. As for **Claim 10** (see objection above), Kim et al., disclose, the image sensor of Claim 7, wherein the adjustments to the auto black expansion circuitry are made in between field of pixel signals.

The Applicant defines, on pages 2 (lines 16), 3 (lines 15 and 16), 4 (line 3), 8 (line 18), 9 (lines 16 and 17), 10 (lines 21 and 22), and 12(line 1), that a "field of pixel signals" corresponds to an image signal, or rather a "sensed image" or a "scene". Thus, Kim et al. teach that adjustments to the black level calibration are made on image signals, as stated in column 3 (lines 14 – 18), and thus, are made between fields of pixel signals.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al.

16. As for **Claim 3**, Kim et al. disclose, the method of Claim 1, wherein the digital control signal comprises n-bits.

Kim et al. teach that the control signal is an n-bit digital control signal, as stated in column 4 (line 9). Kim et al. in no way limit the number of bits included in the digital control signal, and hence, Kim et al. do not specifically disclose an 8-bit digital control signal. However, an 8-bit control signal is commonly known and used in the art and, thus, at the time

the invention was made one with ordinary skill in the art would have been motivated to and it would have been obvious for Kim et al. to have used an 8-bit control signal.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
May 13, 2004

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